

**WHAT IS CLAIMED IS:**

- 1           1.       A method for analyzing input output (I/O) pin arrangements to  
2       determine the effect of differential pair and power and ground pin placement on signal  
3       quality comprising:  
4           constructing an array of pins;  
5           arranging a plurality of differential pairs within the array of pins to provide a  
6           pin arrangement;  
7           exciting each of the differential pairs within the pin arrangement;  
8           monitoring coupled noise on other differential pairs within the pin  
9           arrangement;  
10          analyzing the pin arrangement based upon the monitoring.
- 1           2.       The method of claim 1 wherein the analyzing the pin arrangement  
2       includes:  
3           generating a coupling plot based upon the monitoring; and  
4           determining cumulative coupling based upon the coupling plot.
- 1           3.       The method of claim 1 wherein the pin arrangement includes:  
2       maximally packed differential pairs.
- 1           4.       The method of claim 1 wherein the pin arrangement includes:  
2       power and ground pins as well as differential pairs.
- 1           5.       The method of claim 4 wherein:  
2       the differential pairs, power pins and ground pins are arranged according to a  
3       ratio of eight differential pairs per one power pin and one ground pin.
- 1           6.       The method of claim 4 wherein the pin arrangement includes:  
2       the differential pairs, power pins and ground pins are arranged according to a  
3       ratio of six different pairs per one power pin and one ground pin.

1           7.     The method of claim 4 wherein the pin arrangement includes:  
2           the differential pairs, power pins and ground pins are arranged according to a  
3           ratio of four differential pairs per one power pin and one ground pin.

1           8.     An apparatus for analyzing input output (I/O) pin arrangements to  
2     determine the effect of differential pair and power and ground pin placement on signal  
3     quality comprising:  
4           means for constructing an array of pins;  
5           means for arranging a plurality of differential pairs within the array of pins to  
6           provide a pin arrangement;  
7           means for exciting each of the differential pairs within the pin arrangement;  
8           means for monitoring coupled noise on other differential pairs within the pin  
9           arrangement;  
10          means for analyzing the pin arrangement based upon the monitoring.

1           9.     The apparatus of claim 8 wherein the means for analyzing the pin  
2     arrangement includes:  
3           means for generating a coupling plot based upon the monitoring; and  
4           means for determining cumulative coupling based upon the coupling plot.

1           10.    The apparatus of claim 8 wherein the pin arrangement includes:  
2           maximally packed differential pairs.

1           11.    The apparatus of claim 8 wherein the pin arrangement includes:  
2           power and ground pins as well as differential pairs.

1           12.    The apparatus of claim 11 wherein:  
2           the differential pairs, power pins and ground pins are arranged according to a  
3           ratio of eight differential pairs per one power pin and one ground pin.

1           13.    The apparatus of claim 11 wherein the pin arrangement includes:  
2           the differential pairs, power pins and ground pins are arranged according to a  
3           ratio of six different pairs per one power pin and one ground pin.

1        14.    The apparatus of claim 11 wherein the pin arrangement includes:  
2        the differential pairs, power pins and ground pins are arranged according to a  
3        ratio of four differential pairs per one power pin and one ground pin.

1        15.    An apparatus comprising:  
2        a processor;  
3        a memory coupled to the processor; and  
4        a system for analyzing input output (I/O) pin arrangements to determine the  
5        effect of differential pair and power and ground pin placement on  
6        signal quality, the system being stored on the memory and executing  
7        on the processor, the system including  
8        a constructing module, the constructing module constructing an array  
9        of pins;  
10       an arranging module, the arranging module arranging a plurality of  
11       differential pairs within the array of pins to provide a pin  
12       arrangement;  
13       an exciting module, the exciting module exciting each of the  
14       differential pairs within the pin arrangement;  
15       a monitoring module, the monitoring module monitoring coupled noise  
16       on other differential pairs within the pin arrangement; and,  
17       an analyzing module, the analyzing module analyzing the pin  
18       arrangement based upon the monitoring.

1        16.    The apparatus of claim 15 wherein the analyzing module includes:  
2        a generating module, the generating module generating a coupling plot based  
3        upon the monitoring; and  
4        a determining module, the determining module determining cumulative  
5        coupling based upon the coupling plot.

1        17.    The apparatus of claim 15 wherein the pin arrangement includes:  
2        maximally packed differential pairs.

1        18.    The apparatus of claim 15 wherein the pin arrangement includes:  
2        power and ground pins as well as differential pairs.

1        19.    The apparatus of claim 18 wherein:  
2        the differential pairs, power pins and ground pins are arranged according to a  
3        ratio of eight differential pairs per one power pin and one ground pin.

1        20.    The apparatus of claim 18 wherein the pin arrangement includes:  
2        the differential pairs, power pins and ground pins are arranged according to a  
3        ratio of six different pairs per one power pin and one ground pin.

1        21.    The apparatus of claim 18 wherein the pin arrangement includes:  
2        the differential pairs, power pins and ground pins are arranged according to a  
3        ratio of four differential pairs per one power pin and one ground pin.